IN THE CLAIMS

1. (Currently Amended) A method of preparing operands that are represented in two's complement format for use in binary arithmetic in an electronic device, comprising:

for each operand, determining whether an original value is within a predetermined proximity of a maximum positive/maximum negative value boundary associated with the two's complement format; and

if any of the original operand values is within the predetermined proximity, adjusting all of the original operand values such that ~~rotation~~ cross over from the maximum positive value to the maximum negative value is avoided and to produce respectively corresponding adjusted operand values and providing the adjusted operand values for use in a binary arithmetic operation.

2. (Original) The method of Claim 1, wherein none of the adjusted operand values are within the predetermined proximity of the maximum positive/maximum negative value boundary.

3. (Original) The method of Claim 1, wherein the adjusted operand values require less bits than the respectively corresponding original operand values.

4. (Original) The method of Claim 3, wherein the original operand values require 8 bits and the adjusted operand values

require 7 bits.

5. (Original) The method of Claim 1, wherein said adjusting step includes adding a common value to each of the original operand values to produce the respective adjusted operand values.

6. (Original) The method of Claim 5, wherein the common value is one of 64 and 128.

7. (Original) The method of Claim 1, wherein said adjusting step includes subtracting a common value from each of the original operand values to produce the respective adjusted operand values.

8. (Original) The method of Claim 7, wherein the common value is 64.

9. (Original) The method of Claim 1, wherein the binary arithmetic operation includes an operation performed by an extrinsic block of a turbo decoder.

10. (Original) The method of Claim 9, wherein the operands are state metrics calculated by the turbo decoder for input to the extrinsic block.

11. (Withdrawn) An apparatus for preparing operands that are represented in two's complement format for use in binary arithmetic, comprising:

an input for receiving the operands;

logic coupled to said input for determining, for each operand, whether an original value thereof is within a predetermined proximity of a maximum positive/maximum negative value boundary associated with the two's complement format;

an adjuster coupled to said logic and responsive to a determination by said logic that any of the original operand values is within the predetermined proximity for adjusting all of the original operand values to produce respectively corresponding adjusted operand values; and

an output coupled to said adjuster for providing the adjusted operand values for use in a binary arithmetic operation.

12. (Withdrawn) The apparatus of Claim 11, wherein said logic includes a plurality of AND gates having respective outputs coupled to respective ones of a plurality of OR gates.

13. (Withdrawn) The apparatus of Claim 11, wherein none of the adjusted operand values are within the predetermined proximity of the maximum positive/maximum negative value boundary.

14. (Withdrawn) The apparatus of Claim 11, wherein the

adjusted operand values require less bits than the respectively corresponding original operand values.

15. (Withdrawn) The apparatus of Claim 11, wherein said adjuster is operable for adding a common value to each of the original operand values to produce the respective adjusted operand values.

16. (Withdrawn) The apparatus of Claim 11, wherein said adjuster is operable for subtracting a common value from each of the original operand values to produce the respective adjusted operand values.

17. (Withdrawn) The apparatus of Claim 16, wherein said adjuster is operable for adding a common value to each of the original operand values to produce the respective adjusted operand values.

18. (Currently amended) A maximum a posteriori decoder, comprising:

an alpha block for producing alpha state metrics in two's complement format;

a beta block for producing beta state metrics in two's complement format;

an extrinsic block having an input coupled to said alpha block and said beta block for receiving said alpha state metrics and said beta state metrics as operands, said extrinsic block responsive to said operands for producing extrinsics data; and

said extrinsic block including logic coupled to said input for determining, for each operand, whether an original value ~~thereof~~ is within a predetermined proximity of a maximum positive/maximum negative value boundary associated with the two's complement format, and an adjuster coupled to said logic and responsive to a determination by said logic that any of the original operand values is within the predetermined proximity for adjusting all of the original operand values such that cross over from the maximum positive value to the maximum negative value is avoided and to produce respectively corresponding adjusted operand values for use in producing the extrinsics data.

19. (Original) The decoder of Claim 18, wherein none of the adjusted operand values are within the predetermined proximity of the maximum positive/maximum negative value boundary.

20. (Original) The decoder of Claim 18, wherein the adjusted operand values require less bits than the respectively corresponding original operand values.

21. (Original) The decoder of Claim 18, wherein said adjuster is operable for adding a common value to each of the original operand values to produce the respective adjusted operand values.

22. (Original) The decoder of Claim 18, wherein said adjuster is operable for subtracting a common value from each of the original operand values to produce the respective adjusted operand values.

23. (Original) The decoder of Claim 22, wherein said adjuster is operable for adding a common value to each of the original operand values to produce the respective adjusted operand values.

24. (Currently amended) A decoder, comprising:

a first input for receiving input values;

a first quadrant shifter coupled to the first input; and

the first quadrant shifter including:

a quadrant identifier responsive to the

input values for producing quadrant information of the received input values;

a rotator coupled to the first input;

a rotation selector responsive to the quadrant information provides selection information to the rotator; and

the rotator in response to receiving the selection information rotates the input values to produce corresponding rotated values such that ~~rotation~~ cross over from a maximum positive value to a maximum negative value is avoided.

25. (Previously presented) A decoder as defined in claim 24, wherein the decoder comprises a turbo decoder.

26. (Previously presented) A decoder as defined in claim 25, wherein the input values comprise alpha metrics.

27. (Previously presented) A decoder as defined in claim 25, wherein the input values comprise beta metrics.

28. (Previously presented) A decoder as defined in claim 24, wherein the input values comprise binary values in two's complement format.

29. (Previously presented) A decoder as defined in claim 28, wherein the rotator causes the input values to fall in the first, third or both the first and third quadrants.